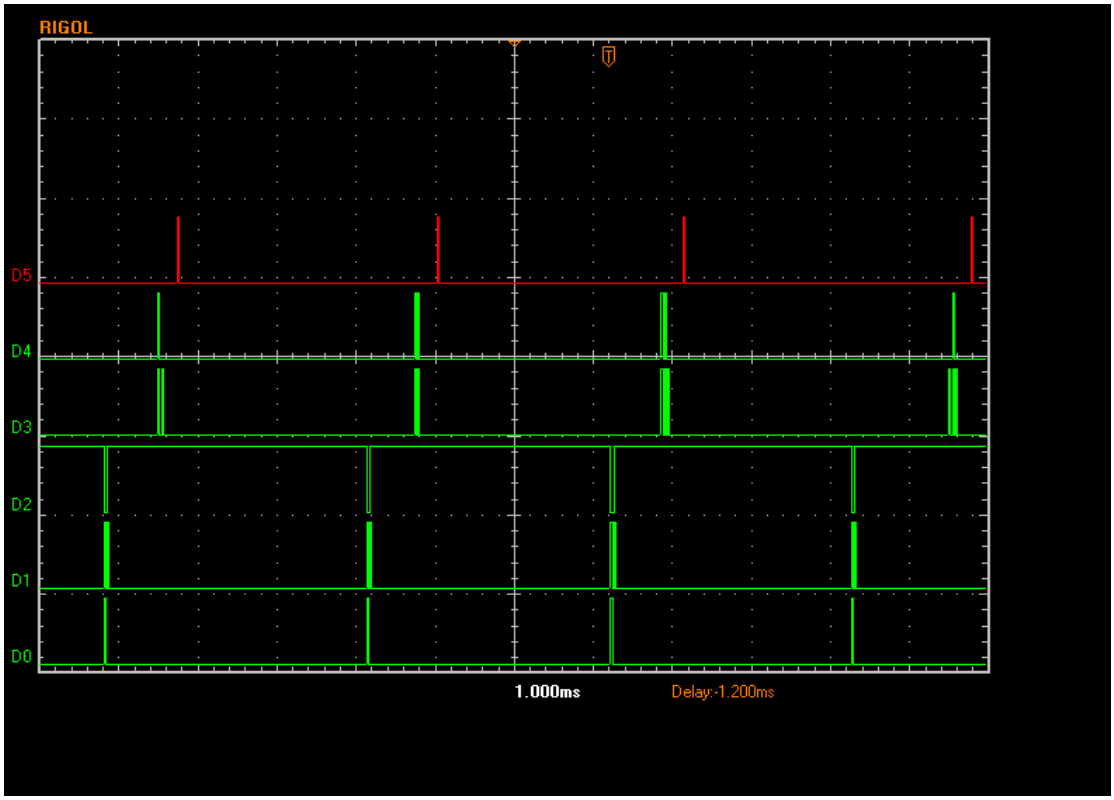
Overall scan summary – 15 August 2010-08-15

The code has been reworked now to use structures for ADC control and device setting in the scan. Decided to stop here for a while

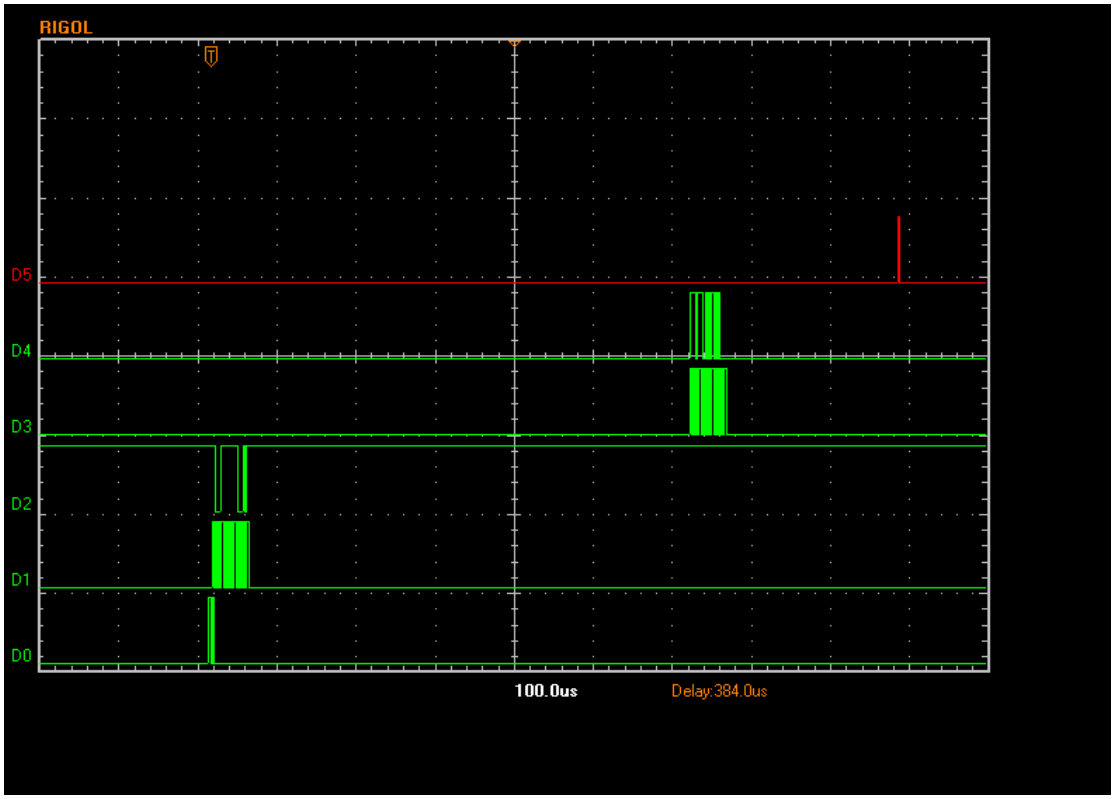
Here is a logic analyser trace of part of a scan. The I/O lines shown are:

D0 = ADC Convert
D1 = ADC clock
D2 = ADC data
D3 = main clock
D4 = DDS data
D5 = DDS FQUD

What is shown here are 3 complete steps in a 400 step trace. Times vary slightly with variations in PC timings and correlation to the 125 usec framing structure of USB but it is just over 3 ms per step, giving an overall scan time of 1.3 seconds for 400 steps averaged over 10 scans.

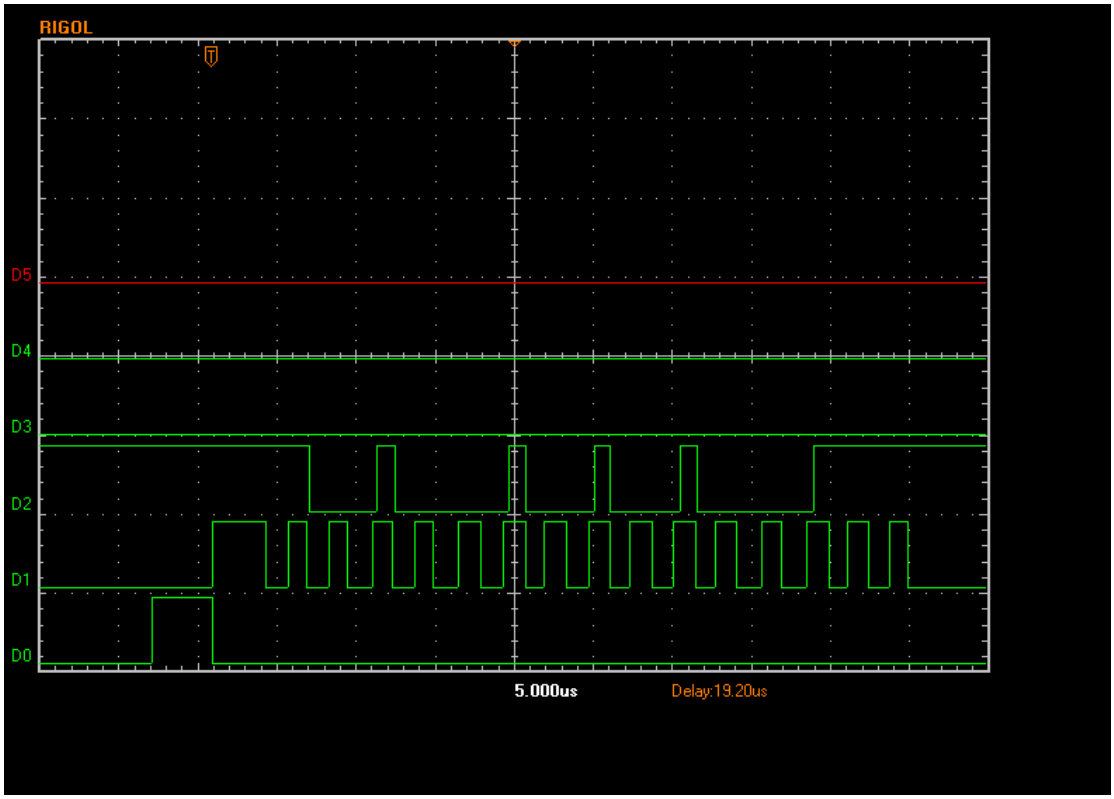


Zooming in on one set of events from ADC convert to DDS setting gives this

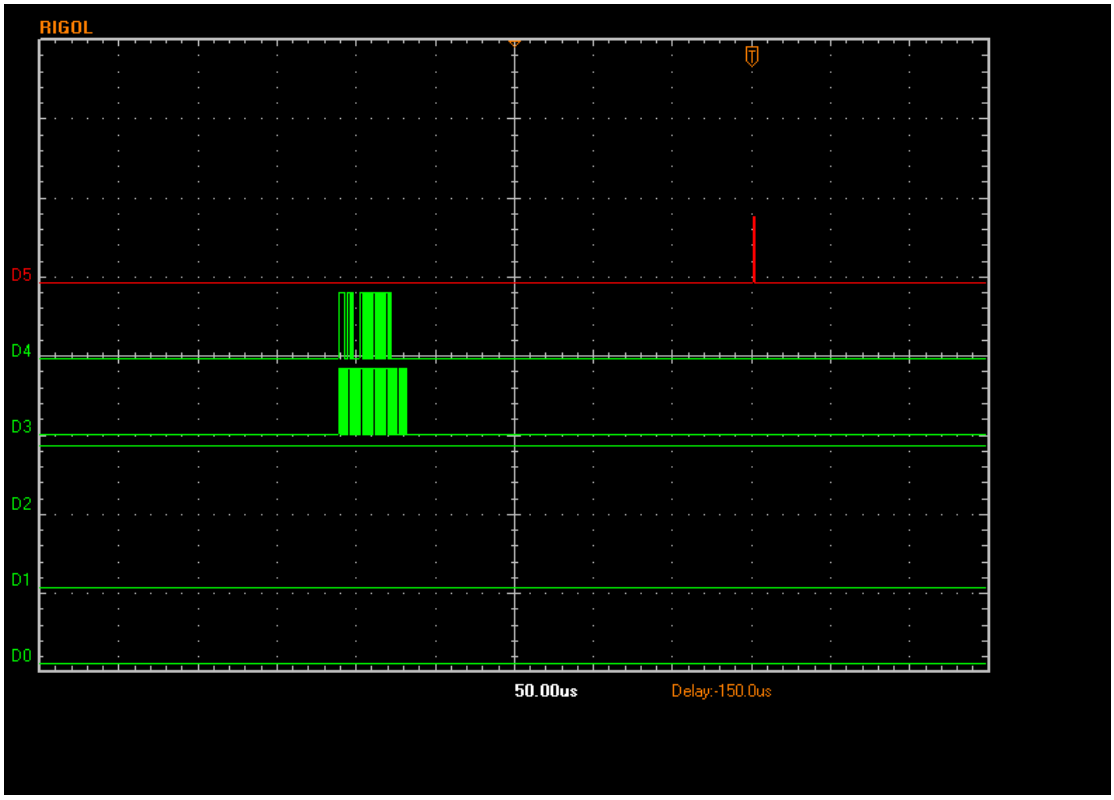


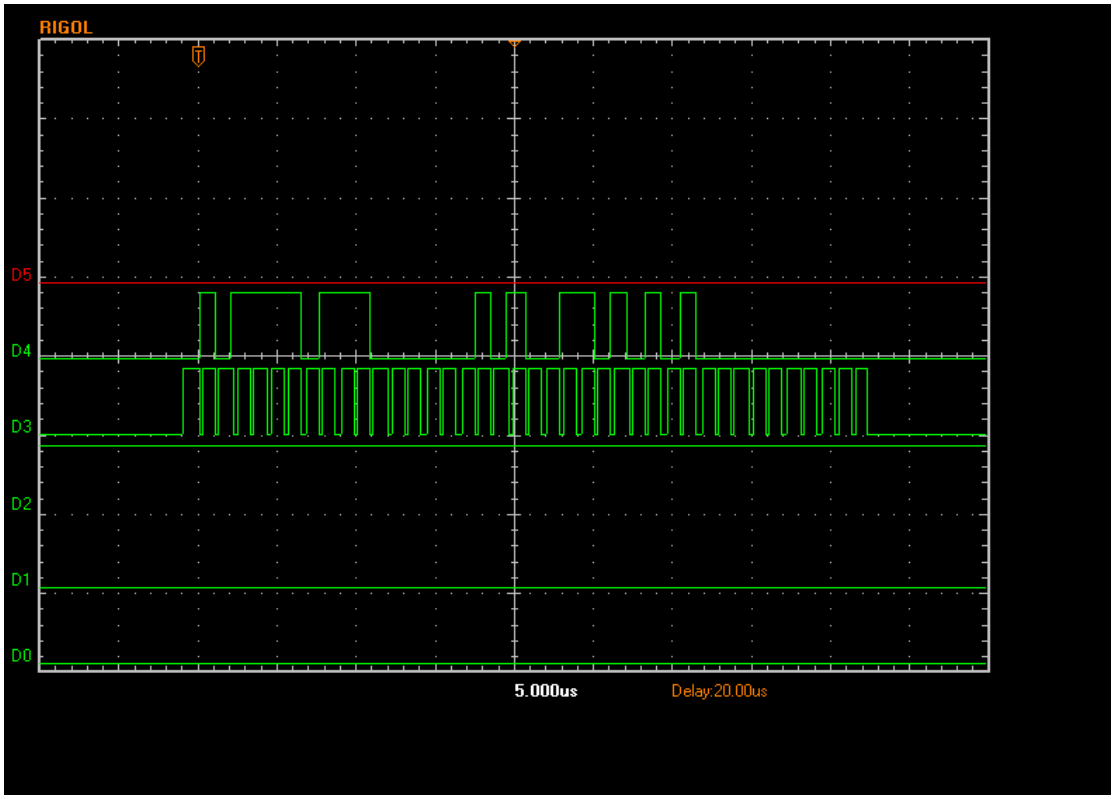
From the perspective of the PC, the time taken to set the DDS is irrelevant as long as it is reasonably fast as this is being handled in parallel to the main PC program running. The only critical timing is the delay from when we ask the ADC to convert (some time prior to the actual conversion above depending on USB framing – anything from 0 to 125 usec) to when it gets the result (probably about 125 usec after the conversion is complete).

Zooming in on the ADC convert gives this



And on the DDS setting these 2 traces




RIGOL
D5
D4
D3
D2
D1
D0
5.000us
Delay:20.00us